IN THE CLAIMS

WHAT IS CLAIMED IS:

1. (Original) A receiver adapted for coupling to a communication medium, said receiver comprising:

   a plurality of PN code generators each having an input signal path and an output signal path;

   load logic coupled to the input signal path of each of the plurality of PN code generators and adapted to receive chips from the communication medium and adapted to pre-load the plurality of PN code generators with information derived from the received chips and adapted to operate the plurality of PN code generators substantially in parallel following pre-loading thereof;

   selection logic coupled to the output signal path of each of the plurality of PN code generators to select a correlated PN code generator from the plurality of PN code generators; and

   a decoder coupled to the selection logic for decoding data received from the communication medium using the correlated PN code generator.

2. (Original) The receiver of claim 1 wherein each of the plurality of PN code generators comprises a Gold code generator.

3. (Previously Amended) The receiver of claim 2 wherein each generator of the plurality of Gold code generators comprises a first *N* bit shift register and second *N* bit shift register and wherein the plurality of Gold code generators comprises 2^N Gold code generators, wherein *N* is the number of shift register stages to hold a Gold code sequence as a value.

4. (Currently Amended) The receiver of claim 3 wherein the load logic comprises:

   first logic, responsive to receipt of a 0 chip value from the communication medium, adapted to load a logic 0 bit value into the first *N* bit shift register and into the second *N* bit shift register of each generator of a first half of the plurality of Gold code generators and adapted to load a logic 1 bit value into the first *N* bit shift register and into the second *N* bit shift register of each generator of a second half of the plurality of ~~the other half of the~~ Gold code generators; and

second logic, responsive to receipt of a 1 chip value from the communication medium, adapted to load a logic 1 bit value into the first *N* bit shift register and to load a logic 0 bit value into the second *N* bit shift register of each generator of the first half of the plurality of Gold code generators and adapted to load a logic 0 bit value into the first *N* bit shift register and adapted to load a logic 1 bit value into the second *N* bit shift register of each generator of the second half of the plurality of Gold code generators,

wherein the first logic and the second logic are operable to assure all possible combinations of *N* bits are loaded into the first and second *N* bit shift registers of the plurality of Gold code generators.

5. (Previously Amended) The receiver of claim 4 wherein the load logic further comprises:

indexing logic to selectively associate each generator of the plurality of Gold code generators with said first half or with said second half.

6. (Previously Amended) The receiver of claim 3 wherein the load logic comprises:

logic adapted to load the first and second *N* bit shift registers as follows:

let $A_{i,j}$ represent the first *N* bit shift registers of the 2^N generators as a 2^Nx*N* matrix and let $B_{i,j}$ represent the second *N* bit shift registers of the 2^N generators as a 2^Nx*N* matrix where *N* is the number of stages in the Gold code where *i* is the generator index number ranging from 0 to 2^N-1 and *j* is the stage index number ranging from 0 to *N*-1,

let C_0 through C_{N-1} represent the first *N* received chips,

then $A_{i,j}$ values are loaded as:

$$A_{i,N-1-j}[[:]] = \frac{1-(-1)^{floor(i\cdot 2^{-j})}}{2}$$

and $B_{i,j}$ values are loaded as a function of C_j and $A_{i,j}$ as follows:

$C_j[[:]] = 0$	$B_{i,N-1-j}[[:]] = A_{i,N-1-j}$
$C_j[[:]] = 1$	$B_{i,N-1-j}[[:]] = \mathrm{mod}(A_{i,N-1-j} + 1,2)$

where: floor(x) is the integer value of x.

7. (Previously Amended) The receiver of claim 1 wherein the load logic comprises:

feedback logic, responsive to completion of the pre-loading of the plurality of PN code generators, to selectively couple the output signal path of each PN code generator to

the corresponding input signal path of each PN code generator to permit operation of the plurality of PN code generators.

8. (Currently Amended) The receiver of claim 1 wherein the selection logic comprises:

autocorrelation detection logic to determine the autocorrelation level of each of the plurality of PN code generators; and

threshold comparison logic to compare the autocorrelation level of each of the plurality of PN code generators to a predetermined threshold to identify a~~the~~ correlated PN code generator.

9. (Previously Amended) A receiver comprising:

a plurality of Gold code generators operable substantially in parallel, each Gold code generator including a first shift register having *N* stages, and a second shift register having *N* stages, wherein *N* is the number of shift register stages to hold a Gold code sequence as a value;

a selector for selecting a correlated generator from said plurality of Gold code generators to use for decoding of received chips;

a pre-loader coupled to the plurality of Gold code generators for pre-loading the first and second shift registers in each generator prior to operating the plurality of Gold code generators; and

feedback logic, responsive to the pre-loader and associated with each generator, to selectively couple an output of each generator to an input of said each generator.

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Previously Amended) The receiver of claim 9 wherein the selector comprises:

a correlator coupled to an output of each generator to determine the correlation of each generator to a sequence of received chips,

wherein the selector is operable to select a best correlated generator as determined by evaluating the sequence of receiver chips.

14. (Previously Amended) The receiver of claim 13 wherein the correlator comprises:

a threshold comparator that compares the correlation of each generator with a predetermined threshold correlation level.

15. (Previously Amended) The receiver of claim 9 wherein the plurality of Gold code generators comprises:

2^N Gold code generators where N is the number of stages in the first and second shift registers of each generator.

16. (Currently Amended) The receiver of claim 14 wherein the ~~further comprising:~~

~~a~~ pre-loader coupled ~~d~~ to the plurality of Gold code generators for pre-loading the first and second shift registers in each generator prior to operating the plurality of Gold code generators wherein each generator is pre-loaded with a unique pre-load value selected from 2^N possible values where N is the number of stages in the first and second shift registers in said each generator.

17. (Currently Amended) A method operable in a digital communication receiver, the method comprising:

receiving digitally encoded information from a communication medium wherein a PN code is used to spread the information over available communication bandwidth of the communication medium;

operating a plurality of PN code generators substantially in parallel with one another to acquire a correct PN code sequence from the received information, the correct PN code sequence determined by a best correlated PN code generator, wherein each PN code generator includes a first shift register having N stages, and a second shift register having N stages, wherein N is the number of shift register stages to hold a PN code sequence as a value; and

decoding the received information using the best correlated PN code generator.

18. (Currently Amended) The method of claim 17 further comprising:

pre-loading the first and second shift registers in each PN code generator prior to operating said each PN code generator.

19. (Currently Amended) The method of claim 18 wherein the plurality of PN code generators comprises 2^N Gold code generators and wherein the first and second shift registers in each Gold code generator include *N* stages, *N* being the number of shift register stages to hold a Gold code sequence as a value, and wherein the step of pre-loading further comprises:

pre-loading said first and second shift registers of each Gold code generator with a corresponding value of 2^N possible values.

20. (Previously Amended) The method of claim 19 wherein the step of pre-loading further comprises:

deriving for each generator a value for pre-loading from *N* received chips of the received information.

21. (Original) The method of claim 17 further comprising:

selecting the best correlated PN code generator by comparing outputs from each of the plurality of PN code generators with a sequence of chips of the received information.

22. (Currently Amended) An apparatus operable in a digital communication receiver, the apparatus comprising:

receiving means for receiving digitally encoded information from a communication medium wherein a PN code is used to spread the information over available communication bandwidth of the communication medium;

code synchronizer means for operating a plurality of PN code generators substantially in parallel with one another to acquire a correct PN code sequence from the received information, the correct PN code sequence determined by a best correlated PN code generator, wherein each PN code generator includes a first shift register having *N* stages, and a second shift register having *N* stages, wherein *N* is the number of shift register stages to hold a PN code sequence as a value; and

means for decoding received information using the best correlated PN code generator.

23. (Currently Amended) The apparatus of claim 22 further comprising:

load logic means for pre-loading the first and second shift registers in each PN code generator prior to operating said each PN code generator.

24. (Currently Amended) The apparatus of claim 23 wherein the plurality of PN code generators comprises 2^N Gold code generators and wherein the first and second shift registers in each Gold code generator include N stages, N being the number of shift register stages to hold a Gold code sequence as a value, and wherein the load logic means ~~further~~ comprises:

Gold code load logic means for pre-loading said first and second shift registers of each Gold code generator with a corresponding value of 2^N possible values.

25. (Currently Amended) The apparatus of claim 24 wherein the Gold code load logic means ~~further~~ comprises:

means for deriving for each generator a value for pre-loading from N received chips of the received information.

26. (Previously Amended) The apparatus of claim 22 further comprising:

selection logic means for selecting the best correlated PN code generator by comparing outputs from each of the plurality of PN code generators with a sequence of chips of the received information.